SLLS047L - FEBRUARY 1989 - REVISED MARCH 2004

- Meets or Exceeds TIA/EIA-232-F and ITU **Recommendation V.28**
- **Operates From a Single 5-V Power Supply** With 1.0-μF Charge-Pump Capacitors
- Operates Up To 120 kbit/s
- Two Drivers and Two Receivers
- ±30-V Input Levels
- Low Supply Current . . . 8 mA Typical
- **ESD Protection Exceeds JESD 22** - 2000-V Human-Body Model (A114-A)
- **Upgrade With Improved ESD (15-kV HBM)** and 0.1-μF Charge-Pump Capacitors is **Available With the MAX202**
- **Applications**
 - TIA/EIA-232-F, Battery-Powered Systems, Terminals, Modems, and Computers

MAX232 . . . D, DW, N, OR NS PACKAGE MAX232I...D. DW. OR N PACKAGE (TOP VIEW) 16 V_{CC} V_{S+} [] 2 15 **∏** GND C1− [3 14 T10UT C2+ [] 4 13 R1IN C2− ¶ 5 12 R10UT V_{S−} [] 6 11 T1IN T20UT [] 7 10 T2IN R2IN **1** 8 9 R20UT

description/ordering information

The MAX232 is a dual driver/receiver that includes a capacitive voltage generator to supply TIA/EIA-232-F voltage levels from a single 5-V supply. Each receiver converts TIA/EIA-232-F inputs to 5-V TTL/CMOS levels. These receivers have a typical threshold of 1.3 V, a typical hysteresis of 0.5 V, and can accept ±30-V inputs. Each driver converts TTL/CMOS input levels into TIA/EIA-232-F levels. The driver, receiver, and voltage-generator functions are available as cells in the Texas Instruments LinASIC™ library.

ORDERING INFORMATION

TA	PAC	KAGE [†]	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
	PDIP (N)	Tube of 25	MAX232N	MAX232N	
	COIC (D)	Tube of 40	MAX232D	MANAGO	
000 1- 7000	SOIC (D)	Reel of 2500	MAX232DR	MAX232	
0°C to 70°C	0010 (DW)	Tube of 40	MAX232DW	MANAGO	
	SOIC (DW)	Reel of 2000	MAX232DWR	MAX232	
	SOP (NS)	Reel of 2000	MAX232NSR	MAX232	
	PDIP (N)	Tube of 25	MAX232IN	MAX232IN	
	0010 (D)	Tube of 40	MAX232ID	MANAGON	
-40°C to 85°C	SOIC (D)	Reel of 2500	MAX232IDR	MAX232I	
	SOIC (DW)	Tube of 40	MAX232IDW	MAX232I	
	SOIC (DW)	Reel of 2000	MAX232IDWR	IVIAA2321	

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

LinASIC is a trademark of Texas Instruments.



Function Tables

EACH DRIVER

INPUT TIN	OUTPUT TOUT
L	Н
Н	L

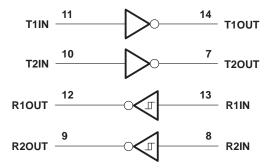
H = high level, L = low level

EACH RECEIVER

INPUT RIN	OUTPUT ROUT
L	Н
Н	L

H = high level, L = low level

logic diagram (positive logic)





SLLS047L - FEBRUARY 1989 - REVISED MARCH 2004

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input supply voltage range, V _{CC} (see Note 1)		0.3 V to 6 V
Positive output supply voltage range, V _{S+}		$V_{CC} - 0.3 \text{ V to } 15 \text{ V}$
Negative output supply voltage range, V _S		0.3 V to -15 V
Input voltage range, V _I : Driver	0	0.3 V to V_{CC} + 0.3 V
Receiver		±30 V
Output voltage range, VO: T1OUT, T2OUT	V _{S-} -0	$0.3 \text{ V to V}_{S+} + 0.3 \text{ V}$
R10UT, R20UT	C	$0.3 \text{ V to V}_{CC} + 0.3 \text{ V}$
Short-circuit duration: T1OUT, T2OUT		Unlimited
Package thermal impedance, θ _{JA} (see Notes 2 and 3):	: D package	73°C/W
	DW package	57°C/W
	N package	67°C/W
	NS package	64°C/W
Operating virtual junction temperature, T _J		150°C
Storage temperature range, T _{stg}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltages are with respect to network GND.
 - 2. Maximum power dissipation is a function of $T_J(max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
 - 3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			MIN	NOM	MAX	UNIT
VCC	Supply voltage		4.5	5	5.5	V
VIH	High-level input voltage (T1IN,T2IN)		2			V
V_{IL}	Low-level input voltage (T1IN, T2IN)				8.0	V
R1IN, R2IN	Receiver input voltage				±30	V
т.	Operating free air temperature	MAX232	0		70	°C
TA	Operating free-air temperature	MAX232I	-40		85	-0

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 4)

	PARAMETER	TEST CONDITIONS			TYP‡	MAX	UNIT
Ic	CC Supply current	V _{CC} = 5.5 V, T _A = 25°C	All outputs open,		8	10	mA

 $[\]ddagger$ All typical values are at V_{CC} = 5 V and T_A = 25°C.

NOTE 4: Test conditions are C1–C4 = 1 μ F at V_{CC} = 5 V \pm 0.5 V.



DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (see Note 4)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Vон	High-level output voltage	T1OUT, T2OUT	$R_L = 3 \text{ k}\Omega \text{ to GND}$	5	7		V
VOL	Low-level output voltage‡	T1OUT, T2OUT	$R_L = 3 \text{ k}\Omega \text{ to GND}$		-7	-5	V
r _O	Output resistance	T1OUT, T2OUT	$V_{S+} = V_{S-} = 0, V_{O} = \pm 2 \text{ V}$	300			Ω
IOS§	Short-circuit output current	T1OUT, T2OUT	$V_{CC} = 5.5 \text{ V}, \qquad V_{O} = 0$		±10		mA
IIS	Short-circuit input current	T1IN, T2IN	V _I = 0			200	μΑ

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

NOTE 4: Test conditions are C1–C4 = 1 μ F at V_{CC} = 5 V \pm 0.5 V.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$ (see Note 4)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Driver slew rate	R_L = 3 kΩ to 7 kΩ, See Figure 2			30	V/µs
SR(t)	Driver transition region slew rate	See Figure 3		3		V/µs
	Data rate	One TOUT switching		120		kbit/s

NOTE 4: Test conditions are C1–C4 = 1 μ F at V_{CC} = 5 V \pm 0.5 V.

RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (see Note 4)

PARAMETER			TEST C	MIN	TYP [†]	MAX	UNIT	
VOH	High-level output voltage	R1OUT, R2OUT	$I_{OH} = -1 \text{ mA}$		3.5			V
VOL	Low-level output voltage [‡]	R1OUT, R2OUT	$I_{OL} = 3.2 \text{ mA}$				0.4	V
V _{IT+}	Receiver positive-going input threshold voltage	R1IN, R2IN	V _{CC} = 5 V,	T _A = 25°C		1.7	2.4	٧
V _{IT} _	Receiver negative-going input threshold voltage	R1IN, R2IN	V _{CC} = 5 V,	T _A = 25°C	0.8	1.2		٧
V _{hys}	Input hysteresis voltage	R1IN, R2IN	V _{CC} = 5 V		0.2	0.5	1	V
rį	Receiver input resistance	R1IN, R2IN	V _{CC} = 5,	$T_A = 25^{\circ}C$	3	5	7	kΩ

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Note 4 and Figure 1)

	PARAMETER					
tPLH(R)	Receiver propagation delay time, low- to high-level output	500	ns			
tPHL(R)	Receiver propagation delay time, high- to low-level output	500	ns			

NOTE 4: Test conditions are C1–C4 = 1 μ F at V_{CC} = 5 V \pm 0.5 V.



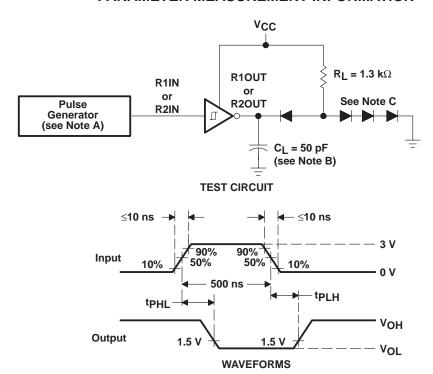
[‡]The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for logic voltage

[§] Not more than one output should be shorted at a time.

[‡]The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.

NOTE 4: Test conditions are C1–C4 = 1 μ F at V_{CC} = 5 V \pm 0.5 V.

PARAMETER MEASUREMENT INFORMATION

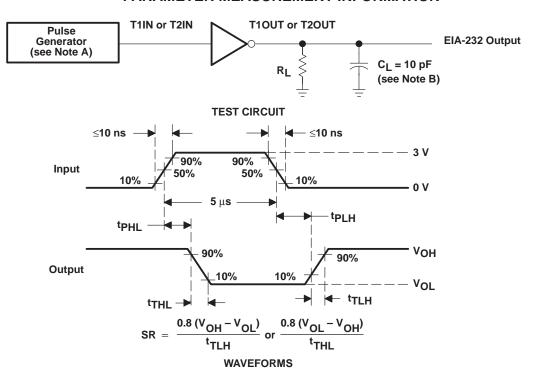


NOTES: A. The pulse generator has the following characteristics: $Z_0 = 50 \Omega$, duty cycle $\leq 50\%$.

- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N3064 or equivalent.

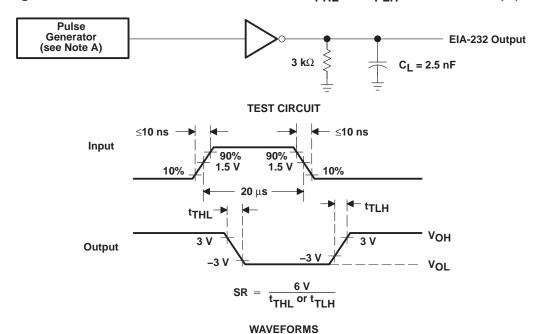
Figure 1. Receiver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurements

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The pulse generator has the following characteristics: $Z_0 = 50 \Omega$, duty cycle $\leq 50\%$.
 - B. C_L includes probe and jig capacitance.

Figure 2. Driver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurements (5-μs Input)

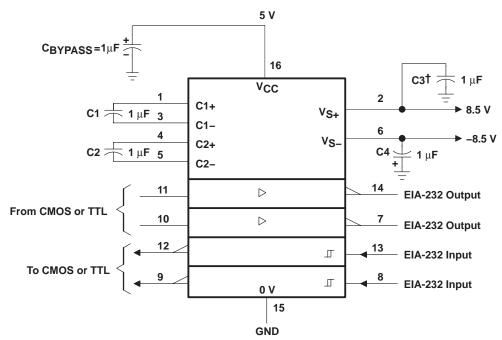


NOTE A: The pulse generator has the following characteristics: $Z_O = 50 \Omega$, duty cycle $\leq 50\%$.

Figure 3. Test Circuit and Waveforms for t_{THL} and t_{TLH} Measurements (20-μs Input)



APPLICATION INFORMATION



†C3 can be connected to VCC or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown. In addition to the 1-µF capacitors shown, the MAX202 can operate with 0.1-µF capacitors.

Figure 4. Typical Operating Circuit







4-Jun-2007

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
MAX232D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232DWE4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232DWRE4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232DWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232ID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IDWE4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IDWRE4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type



PACKAGE OPTION ADDENDUM

4-Jun-2007

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
MAX232INE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
MAX232N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
MAX232NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
MAX232NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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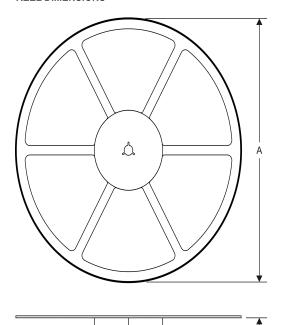
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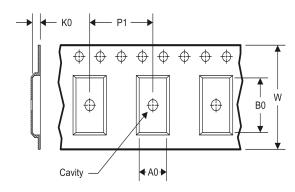
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TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX232DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MAX232DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
MAX232DWRG4	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
MAX232IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MAX232IDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
MAX232NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MAX232DR	SOIC	D	16	2500	346.0	346.0	33.0
MAX232DWR	SOIC	DW	16	2000	366.0	364.0	50.0
MAX232DWRG4	SOIC	DW	16	2000	346.0	346.0	33.0
MAX232IDR	SOIC	D	16	2500	333.2	345.9	28.6
MAX232IDWR	SOIC	DW	16	2000	366.0	364.0	50.0
MAX232NSR	SO	NS	16	2000	346.0	346.0	33.0

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDS0-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



DW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



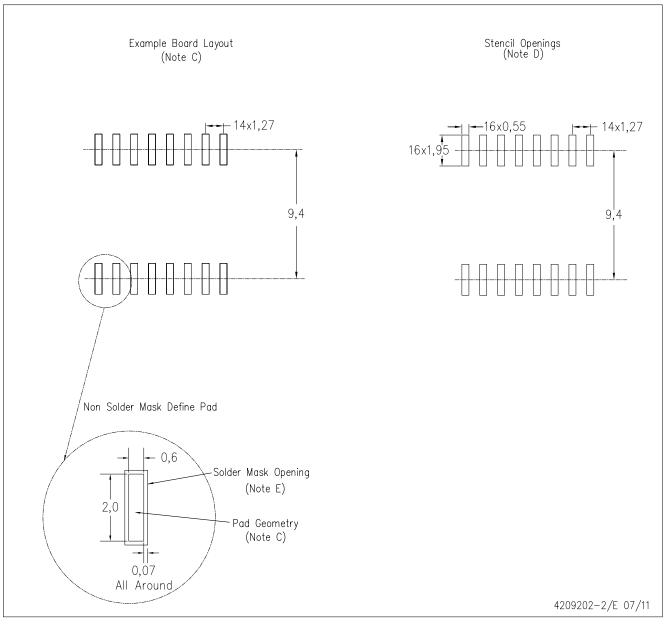
NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AA.



DW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC—7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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Applications

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